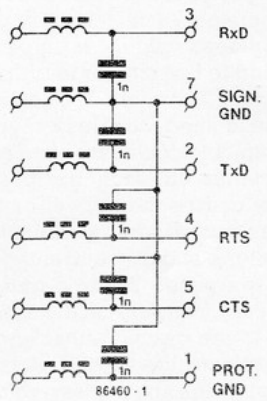
38 filtered connector

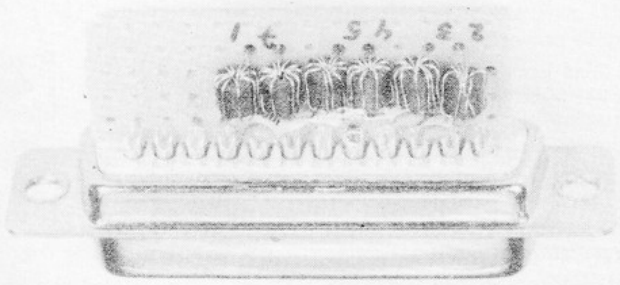
Computers and computer-driven peripherals are notorious sources of RF interference, and receiver jamming may occur at frequencies well above 100 MHz, even though the computer is said to run at a mere 16 MHz or so. The cause of this problem lies in the very fast pulse rise time of the switching and timing signals internal and/or external to the computer system and its peripherals, which are often located well away from one another (printer, modem, mass storage).

Much of the interference originating from long peripheral wiring systems may be suppressed quite effectively by inserting simple low-pass filters in the signal lines for data and handshaking. The proposed L-C filters are composed of small (3 mm) ferrite beads with 10 turns of 0.2 mm (36 SWG) enamelled copper wire, plus a ceramic 1 nF capacitor; the coil inductance is about 80 µH, which gives a cut-off frequency of about 60 kHz (120 Kbaud).

The filters are mounted on a small piece of veroboard which may be cut and filed to fit into a standard D-connector housing. Other cut-off frequencies may be defined by modifying the small coils; inductance is proportional to the square of the number of turns, while constructors boasting of good (near) eyesight and lots of patience may endeavour to use thin (0.05 mm) copper wire to run through the beads. However, the L-C ratio as given should not be modified.

In conclusion, it should be noted that a filtered connector dimensioned for, say, 10 kHz, should not be connected to a high frequency (20 MHz) computer output, since the excessively high capacitive load may cause damage to the line driver IC. *(JB)*





39 random lights controller

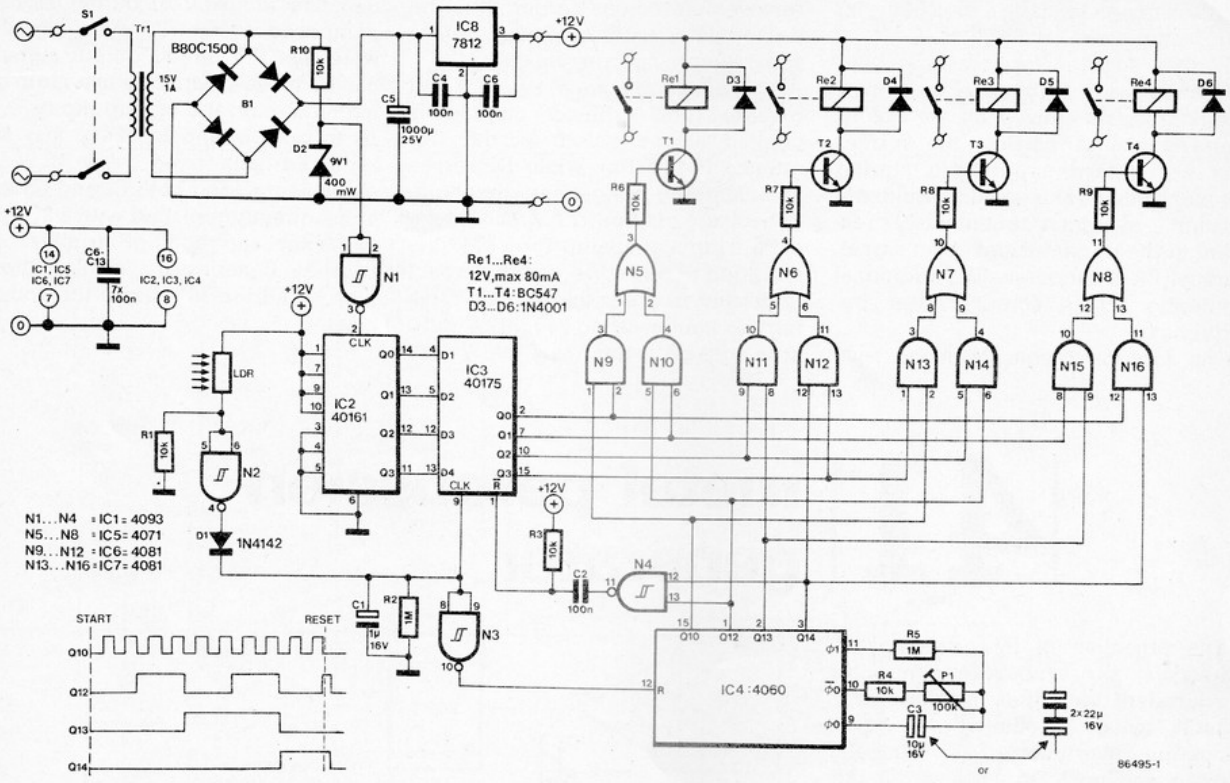
Unfortunately, we are all well aware that the annual holiday season is an anxious time for many people, since they worry about leaving the home unattended and therefore liable to be visited by burglars and/or hooligans. Right now is, therefore, an ideal time to construct this circuit before you leave your home and all of your highly-valued property.

It goes without saying that simulating one's presence in the home may be accomplished by having some electronic or mechanical timer device switch on a number of lights when it grows dark, merely keeping them on until a fixed time interval has lapsed. The potential housebreaker, however, may soon detect the regular pattern that occurs every evening, encouraging him to embark on his nefarious activities, since he realizes he is dealing with a harmless timer rather than persons in the home.

This circuit, while also being a timer, offers a better simulation of human activity, since it automatically arranges for a number of lights to be switched on and off in an apparently random manner, which gives the burglar the impression that there are people at home. In actual fact, the lights pattern is pseudo-random, but 16 possible configurations are bound to ensure sufficient diversity to keep your mind at ease and that of the attentive burglar quite puzzled for at least a few weeks.

And now for the operational principles of this easy-to-build circuit. The evening's specific lights configuration is determined by the four-bit logic code supplied by counter IC_2 at the moment it becomes dark. Since this never happens at precisely the same time every evening, IC_2 may be considered as a four-bit (1 of 16) random code-generator. Whenever the LDR fails to detect the presence of daylight, the output of N_2 goes high, and D_1 charges C_1. Meanwhile, N_1 constantly applies 100 Hz pulses to the input of counter IC_2. When the voltage across C_1 and R_2 has risen to a level, sufficiently high to be recognized as a logic one by the clock input of quad latch IC_3, the four-bit counter code is latched and transferred to the $Q_0 \ldots Q_3$ outputs of IC_3. In addition, N_3 simultaneously enables IC_4 to start counting and dividing its on-chip generated clock signal.

The latch (IC_3) and counter (IC_4) outputs are combined in AND gates $N_9 \ldots N_{16}$. The oscillator parts to IC_4



R_4-P_1-R_5-C_3 (the latter is a bipolar type which may be substituted by two series-connected electrolytic capacitors) have been dimensioned such that output Q_{10} produces 15-minute long, 50% duty factor pulses; this interval may be set accurately by means of P_1. Since IC_4 is a binary (2^n) divider, outputs Q_{12}, Q_{13} and Q_{14} provide pulse period times of 60, 120 and 240 minutes respectively. Whether or not these pulses can appear at the outputs of $N_9 \ldots N_{16}$ depends on the current logic level of each of the associated latch outputs $Q_0 \ldots Q_3$. The AND gate outputs have een paired in four OR gates $N_5 \ldots N_8$; therefore N_5 and N_7 may supply either 15, 60, or 75-minute intervals, while N_6 and N_8 cater for relay-on times of either 60, 120, or 180 minutes; longer times (e.g. 360 minutes) are not feasible since N_4 resets IC_3, five hours (Q_{12} *AND* Q_{14} = *60+240 = 300 min.*) after it fell dark at the LDR mounting position.

It is seen that Re_1 and Re_3 are therefore best used for those lights that can be expected to go on and off for relatively short periods during the evening, while Re_2 and Re_4 are energized for longer times at later hours that same night.

Finally, the inset timing diagram illustrates the pulse sequence relevant to the four relay outputs.

AR

synchronization separator 40

Obtaining TV synchronization pulses from a composite video signal generally presents few problems, as can be concluded from the relative simplicity of sync separator circuits in colour- as well as monochrome TV sets. However, if TV sync pulses are to be used for further processing in digital circuits, the commonly encountered sync separator fails to meet the requirements for output pulse definition and "cleanness". Thus, the separation level needs to be accurately defined in order to prevent blanking rather than synchronization pulses to appear at